Docket No.: 064965-0057

OIPE
MAY 27 2005

CoFC

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 20277
 :
John CHIANG, et al. : Confirmation Number: 1446
 :
Application No.: 09/304,964 :
Patent No.: 6,895,015 B1 : Group Art Unit: 2667
 :
Filed: May 05, 1999 : Examiner: YAO, Kwang Bin
 :
For: DYNAMIC TIME SLOT ALLOCATION IN INTERNAL RULES CHECKER
SCHEDULER

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 CFR 1.322

Mail Stop Box 4
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate
JUN 0 6 2005
of Correction

Sir:

In reviewing the above-identified patent, a printing error was discovered therein requiring

correction in order to conform the Official Record in the application.

The error noted is set forth on the two attached copies of form PTO-1050 Rev. 2-93 in the

manner required by the Commissioner's Notice.

Specifically, **Under "What is Claimed is:", Claim 13, Column 12, Line 28, after the**

word queue insert – if the first data queue –. For your immediate reference a photocopy of

the Amendment filed on November 17, 2004.

The change requested herein occurred as a result of printing the Letters Patent and the

Certificate should be issued without expense under Rule 322 of the Rules of Practice.

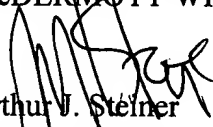Accordingly, Applicants request issuance of the Certificate of Correction.

JUN 0 9 2005

Please charge any shortage in fees due in connection with the filing of this paper to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Arthur J. Steiner
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600 13th Street, N.W.
Washington, DC 20005-3096
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Facsimile: 202.756.8087
Date: May 27, 2005

**Please recognize our Customer No. 20277
as our correspondence address.**

JUN 0 9 2005

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.   : 6895015 B1
DATED   : [case_issue_date]
INVENTOR(S) : John CHIANG, et al.

It is certified that error appears in the above-identified patent and that said Letter Patent is hereby corrected as shown below:

Under "What is Claimed is:",

Claim 13, Column 12, Line 28, after the word queue insert – if the first data queen --

---

MAILING ADDRESS OF SENDER:
McDermott Will & Emery LLP
600 13th Street, NW
Washington, DC 20005
USA

PATENT NO.
6,895,015 B1

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FORM PTO 1050 (Rev. 2-93)

JUN 0 9 2005

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6895015 β|
DATED   : [case_issue_date]
INVENTOR(S) : John CHIANG, et al.

It is certified that error appears in the above-identified patent and that said Letter Patent is hereby corrected as shown below:

Under "What is Claimed is:",

Claim 13, Column 12, Line 28, after the word queue insert – if the first data queen --

---

MAILING ADDRESS OF SENDER:
McDermott Will & Emery LLP
600 13th Street, NW
Washington, DC 20005
USA

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6,895,015 β |

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FORM **PTO 1050** (Rev. 2-93)

JUN 0 9 2005

Docket No.: 64965-057

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
	:	
John CHIANG, et al.	:	Confirmation Number: 1446
	:	
Application No.: 09/304,964	:	Group Art Unit: 2664
	:	
Filed: May 5, 1999	:	Examiner: K.B. Yao
	:	

For: DYNAMIC TIME SLOT ALLOCATION IN INTERNAL RULES CHECKER SCHEDULER

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Amendment is submitted pursuant to 37 CFR 1.196(b) in response to a new ground of

rejection set forth in the Decision on Appeal mailed on September 24, 2004.

IN THE CLAIMS

Claim 1 (cancelled).

2.   (Previously presented) A multiport data communication system for switching data packets between ports, the data communication system comprising:

a plurality of receive ports for receiving data packets,

a decision making engine responsive to the received data packets for controlling transmission of the received data packets to at least one selected transmit port,

the decision making engine including:

a plurality of queuing devices corresponding to the plurality of the receive ports for queuing data blocks representing the data packets received by the corresponding receive ports,

logic circuitry for receiving the data blocks from the plurality of queuing devices in successive time slots to identify the at least one selected transmit port for each data packet,   and

a scheduler interacting with the plurality of queuing devices for dynamically allocating each of the time slots to one of the plurality of queuing devices in accordance with data traffic at the corresponding receive ports,

wherein the scheduler is configured to receive a request for a time slot from a queuing device of the plurality of queuing devices when the queuing device holds data to be processed by the logic circuitry.

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3.   (Original)   The system of claim 2, wherein each of the plurality of the queuing devices is assigned with at least one of the time slots in each scheduling cycle.

4.   (Original)   The system of claim 3, wherein the scheduler is configured to allocate a first time slot assigned to a first queuing device to a second queuing device if no request for a time slot is received from the first queuing device.

5.   (Original)   The system of claim 4, wherein the second queuing device is assigned with a second time slot following the first time slot.

6.   (Original)   The system of claim 5, wherein the scheduler is configured to allocate the first time slot to a third queuing device if no request for a time slot is received from the second queuing device.

7.   (Original)   The system of claim 6, wherein the third queuing device is assigned with a third time slot following the second time slot.

8.   (Previously presented) A multiport data communication system for switching data packets between ports, the data communication system comprising:

a plurality of receive ports for receiving data packets,

a decision making engine responsive to the received data packets for controlling

transmission of the received data packets to at least one selected transmit port,

the decision making engine including:

a plurality of queuing devices corresponding to the plurality of the receive ports for queuing

data blocks representing the data packets received by the corresponding receive ports,

logic circuitry for receiving the data blocks from the plurality of queuing devices in

successive time slots to identify the at least one selected transmit port for each data packet, and

a scheduler interacting with the plurality of queuing devices for dynamically allocating each

of the time slots to one of the plurality of queuing devices in accordance with data traffic at the

corresponding receive ports,

wherein the logic circuitry comprises ingress rules logic for receiving the data block to

check whether the corresponding data packets are received with an error.

9.   (Original)   The system of claim 8, wherein the logic circuitry further comprises

source address lookup logic for comparing a source address of the data packets with a preset source

address.

10.   (Original)   The system of claim 9, wherein the logic circuitry further comprises

destination address lookup logic for comparing a destination address of the data packets with a

preset destination address.

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11.   (Original)   The system of claim 10, wherein the logic circuitry further comprises egress rules logic for producing a port vector identifying the at least one selected transmit port.

Claim 12 (cancelled)

13.   (Currently amended)   In a communication system having a plurality of receive ports, at least one transmit port, and a decision making engine for controlling data forwarding between ~~the~~ a receive port <u>of said plurality of receive ports</u> and the at least one transmit port, a method of data processing comprising the steps of:

placing data blocks representing received data packets in a plurality of data queues corresponding to the plurality of the receive ports,

transferring the data queues in successive time slots to logic circuitry for determining the at least one transmit port, and

dynamically allocating the time slots to the data queues in accordance with data traffic at the corresponding receive ports,

wherein <u>the time slots assigned to the data queues representing underloaded receive ports are dynamically allocated to the data queues representing overloaded receive ports</u> ~~a data queue representing each of the receive ports is assigned with at least one of the time slots~~.

14.   (Original)   The method of claim 13, wherein a first time slot assigned to a first data queue is allocated to the first data queue if the first data queue contains data to be processed.

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15.   (Original)   The method of claim 14, wherein the first time slot is allocated to a second data queue if the first data queue does not contain data to be processed.

16.   (Original)   The method of claim 15, wherein the second data queue is assigned with a second time slot following the first time slot.

17.   (Original)   The method of claim 16, wherein the first time slot is allocated to a third data queue if the first and second data queues do not contain data to be processed.

18.   (Original)   The method of claim 17, wherein the third data queue is assigned with a third time slot following the second time slot.

REMARKS

Claims 2-11, and 13-18 are pending. Claims 1 and 12 are cancelled.

The outstanding rejection of claims 2-11 and 13-18 under 35 U.S.C. 102 as being anticipated by Wu has been reversed.

Claims 13-18 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

In response, claim 13 has been amended to change the words "the receive port" in lines 2-3 to —a receive port of said plurality of receive ports-- to overcome the antecedent problem.

Further, the limitation "a data queue representing each of the receive ports is assigned with at least one of the time slots" has been deleted. Instead, claim 13 recites that the time slots assigned to the data queues representing underloaded receive ports are dynamically allocated to the data queues representing overloaded receive ports.

As indicated in the Decision on Appeal, Wu does not disclose the plurality of queuing devices corresponding to the plurality of receive ports. Hence, the reference does not disclose the steps of:

-placing data blocks representing received data packets in a plurality of data queues corresponding to the plurality of the receive ports; and

-dynamically allocating the time slots to the data queues in accordance with data traffic at the corresponding receive ports,

wherein the time slots assigned to the data queues representing underloaded receive ports are dynamically allocated to the data queues representing overloaded receive ports, as claim 13 recites.

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Accordingly, claims 13-18 are defined over the reference.

In view of the foregoing, and in summary, claims 2-11 and 13-18 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Date: November 17, 2004

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Applicant: John CHIANG, et al.

Title: DYNAMIC TIME SLOT ALLOCATION IN INTERNAL RULES CHECKER SCHEDULER

Docket No. 64965-057

Serial/Reg./Patent No. 09/304,964

Date Sent: 11/17/2004

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New Patent App ☐ Utility ☐ Design ☐ Cont ☐ CIP ☐ Div. ☐ PCT ☐ RCE ☐ Prov

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